IN THE CLAIMS

Claims 6-16 were pending. Claims 8 and 13 have been canceled without prejudice. Claims 6, 10-11, and 15 have been amended. Claims 6-7, 9-12, and 14-16 remain pending. A complete list of claims is presented below with amendments marked up:

Current Listing of Claims:

1.-5. (Canceled).

6. (Currently amended) An apparatus comprising:

a variable delay device having an output, a first input, and a second input; and

a detector having a first input, a second input, and an output, the first input of the detector being coupled to the output of the variable delay device to receive a first clock signal, and the output of the detector being coupled to the second input of the variable delay device to cause the variable delay device to adjust the first clock signal to align an edge of the first clock signal with a center of a data packet, wherein the data packet is input to the second input of the detector.

7. (Original) The apparatus of claim 6, further comprising a clock generator coupled to the first input of the variable delay device to provide a second clock signal to the variable delay device, which generates the first clock signal from the second clock signal.

8. (Canceled).

9. (Original) The apparatus of claim 6, wherein the variable delay device comprises a delay line.

10. (Currently amended) An apparatus comprising: ~~The apparatus of claim 6,~~

a variable delay device having an output, a first input, and a second input; and

a detector having a first input, a second input, and an output, the first input of the detector being coupled to the output of the variable delay device to receive a first clock signal, and the output of the detector being coupled to the second input of the variable delay device to cause the variable delay device to adjust the first clock signal to align an edge of the first clock signal with a center of a data packet, wherein the detector comprises a quadrature phase detector.

11. (Currently amended) A system comprising:

a plurality of dynamic random access memory (DRAM) devices;

a bus; and

a memory controller comprising:

a variable delay device having an output, a first input, and a second input; and

a detector having a first input, a second input, and an output, the first input of the detector being coupled to the output of the variable delay device to receive a first clock signal, and the output of the detector being coupled to the second input of the variable delay device to cause the variable delay device to adjust the first clock signal to

align an edge of the first clock signal with a center of a data packet, wherein the data packet is input to the second input of the detector from one or more of the plurality of DRAM devices via the bus.

12. (Original) The system of claim 11, further comprising a clock generator coupled to the first input of the variable delay device to provide a second clock signal to the variable delay device, which generates the first clock signal from the second clock signal.

13. (Canceled).

14. (Original) The system of claim 11, wherein the variable delay device comprises a delay line.

15. (Currently amended) [[The]] A system ~~of claim 11,~~ comprising:

a plurality of dynamic random access memory (DRAM) devices;

a bus; and

a memory controller comprising:

a variable delay device having an output, a first input, and a second input; and

a detector having a first input, a second input, and an output, the first input of the detector being coupled to the output of the variable delay device to receive a first clock signal, and the output of the detector being coupled to the second input of the variable delay device to cause the variable delay device to adjust the first clock signal to

align an edge of the first clock signal with a center of a data packet, wherein the detector comprises a quadrature phase detector.

16. (Original) The system of claim 11, further comprising a processor coupled to the memory controller.